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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
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Mark Sikkink et al.	)	Examiner: Behzad Peikari
	)	
Serial No.: 09/619,771	)	Group Art Unit: 2186
	)	
Filed: July 20, 2000	)	Docket: 499.078us1
	)	
For: DUAL-BANK FIFO FOR SYNCHRONIZATION OF READ DATA IN DDR SDRAM	)	Customer No. 21186
Assignee: Silicon Graphics, Inc.		

APPELLANTS' BRIEF ON APPEAL

Mail Stop Appeal Brief--Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This brief is presented in support of the Notice of Appeal filed July 13, 2004, from the final rejection of claims 1-20 of the above-identified application. The Final Office Action from which the Appellants hereby appeals was mailed on May 10, 2004.

A check in the amount of $340.00 to cover the fee for filing the appeal brief set forth in 37 C.F.R. § 41.20(b) is enclosed herewith. Please charge any additional required fees or credit overpayment to Deposit Account 19-0743. Appellants respectfully request reversal of the Examiner's rejection of pending claims 1-29.

1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, Silicon Graphics, Inc., a corporation organized and existing under and by virtue of the laws of the State of Delaware, and having an office and place of business at MS 710, 1600 Ampitheatre Parkway, Mountain View, CA, 94043.

2. RELATED APPEALS AND INTERFERENCES

There are no appeals or interferences known to the Appellants which will have a bearing on the Board's decision in the present appeal.

3. STATUS OF THE CLAIMS

Claims 1-29 are pending in the present application, stand under Final Rejection, and are appealed. Claims 1-29 were rejected under 35 USC § 103(a) as being unpatentable over Drako et al. (U.S. 5,371,877) in view of Rust et al., (U.S. 5,699,530), in further view of DeWilde et al. (U.S. 6,434,674).

4. STATUS OF AMENDMENTS

Amendments to claims 1, 11, and 29 were previously presented, but were not entered. The pending amendments are reflected in the marked-up claim set in Appendix I. The advisory action of May 10, 2004, indicated the claims were not entered because adding new limitations, even in the absence of striking any existing claim limitations, would cause restriction requirement issues to arise.

5. SUMMARY OF CLAIMED SUBJECT MATTER

In one example embodiment, a dual bank FIFO memory buffer comprises first and second banks of memory elements operable to buffer memory data. Write control address logic

is operable to store selected memory data in memory elements with selected addresses determined by evaluation of a strobe signal, and write control timing logic is operable to selectively grant write access to the banks of memory elements at predetermined time. The write control timing logic comprises a write pointer associated with each FIFO bank, and is operable to control write access to the associated bank during periods when read data is determined to be valid. Read control logic is operable to read data stored in the first and second banks, and first an second ports connect the dual bank FIFO memory buffer to a memory and to a memory controller, respectively.

Claim 1 recites A dual-bank FIFO as described above, explicitly reciting a first write pointer associated with the first bank and a second write pointer associated with the second bank, each operable to allow received data to be written to their respective banks when the opposite pointer is in a null state. Enabling the first and second write pointers at times dependent on the received strobe signal preamble timing is further recited in claim 1.

Claim 10 recites a dual-bank FIFO buffer as described in the summary paragraph above.

Claim 11 describes a memory controller including substantially the same limitations as claim 1, and 20 describes a computerized information handling system including substantially the same limitations as claim 1.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. Whether claims 1-20 are unpatentable under 35 USC § 103(a) over Drako et al. (U.S. 5,371,877) in view of Rust et al., (U.S. 5,699,530), in further view of DeWilde et al. (U.S. 6,434,674).

7. ARGUMENT

1) The Applicable Law

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). To do that the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would lead an individual to combine the relevant teaching of the references. *Id.* Further, The references when combined must teach or suggest all the claim elements. M.P.E.P. § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir. 1991)).

2) Discussion of the Rejections

I. Whether claims 1-20 are unpatentable under 35 USC § 103(a) over Drako et al. (U.S. 5,371,877) in view of Rust et al., (U.S. 5,699,530), in further view of DeWilde et al. (U.S. 6,434,674).

Drako discusses implementing a dual port FIFO memory by using two banks of single-port RAM, and an apparatus for interleaving reads and writes between banks such that successive writes will be to different memory banks, and such that the memory bank not being written may be read.

Rust describes a circular RAM-based FIFO buffer using interleaved storage and cross pointers. A first RAM bank stores even data, and a second RAM bank stores odd data. A read pointer and a write pointer use shift registers to select the written or read element.

DeWilde is relied upon to show a FIFO buffer 26 located between a memory-coupled MUX 12 and controllers 32 and 34. The FIFO units are described as bi-directional, but little additional detail is given.

The present invention, in contrast, comprises a system for controlling write access to banks in a dual-bank FIFO to ensure written data is valid, where the dual-bank FIFO serves as a buffer between a memory and a memory controller or memory controller interface. More

specifically, the pending claims recite first and second ports for connecting the dual bank FIFO buffer between a memory and a memory controller (Claims 1 and 10), operation within a memory controller as a dual-bank FIFO connected between the data input and the memory and operable to buffer the read data (Claim 11), or coupling a dual-bank FIFO between memory and a memory controller in a computerized information handling system (Claim 20). Each of these claims therefore recites a structure and function of buffering data between a memory and a memory controller or memory controller data input, distinguishing them from combination of Drako, Rust, and DeWilde.

Further, because each of the references solves a problem other than that addressed by the claims of the present invention, and because none of the references teach or suggest combination with the other references to address the subject of buffering data between a dual-bank memory and a memory controller, combination of such reference is improper. The Office Action dated 2/25/2004, paragraph 6 (Allowable Subject Matter) appears to suggest this, but amendments to claims 1, 11, and 20 to further define operation of the write pointers made in response were not entered despite containing only additional elements to previously existing claims because they were stated to raise restriction requirement issues.

Because the cited references fail to teach the structure and function recited in the pending claims of buffering data between a memory and a memory controller or memory controller data input, the pending claims are believed to be distinct from the cited references. Reversal of the rejection of the pending claims 1-29 is therefore respectfully requested.

8. SUMMARY

Appellants believe the claims are in condition for allowance and request withdrawal of the rejections to the pending claims. It is respectfully submitted that the cited art neither anticipates nor renders the claimed invention obvious and that the claimed invention is therefore patentably distinct from the cited art. It is respectfully submitted that claims 1-29 should therefore be allowed, and reversal of the Examiner's rejections of pending claims 1-29 is respectfully requested.

Respectfully submitted,

NORA FEMENIA

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9581

Date Nov. 15 '04 By _____
John M. Dahl
Reg. No. 44,639

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Appeal Brief--Patents, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 15th day of ~~October~~ November, 2004.

~~Your Name~~ Patricia A. Hultman _____
Name Signature

APPENDIX I

The Pending Claims on Appeal

1. (Presently Amended) A dual bank FIFO memory buffer, comprising:

a first bank of memory elements operable to buffer memory data;

a second bank of memory elements operable to buffer memory data;

write control address logic operable to store selected memory data in memory elements with selected addresses;

a first write pointer associated with the first bank of memory elements, the first write pointer operable to allow received data to be written to the first bank of memory elements when a second write pointer is in a null state;

a second write pointer associated with the second bank of memory elements, the second write pointer operable to allow received data to be written to the second bank of memory elements when the first write pointer is in a null state;

write control timing logic operable to selectively grant write access to the banks of memory elements at predetermined times by enabling the first and second write pointers at times dependent on received strobe signal preamble timing;

read control logic operable to read data stored in the first and second banks;

a first port connecting the dual bank FIFO memory buffer to a memory; and

a second port connecting the dual bank FIFO memory buffer to a memory controller.

2. (Previously Amended) The dual bank FIFO memory buffer of claim 1, wherein the memory data is provided by double data rate synchronous dynamic read only memory (DDR SDRAM) operatively connected to the buffer via the first port.

3. (Original) The dual bank FIFO memory buffer of claim 1, wherein the write control address logic is operable to determine an element within a bank of memory elements in which selected memory data is to be stored by evaluating rising and falling edges of a strobe signal.

4. (Original) The dual bank FIFO memory buffer of claim 3, wherein the determination of the element in which selected memory data is to be stored further comprises selection of sequential element addresses during sequential strobe cycles.

5. (Original) The dual bank FIFO memory buffer of claim 1, wherein the write control timing logic comprises a write pointer associated with each FIFO bank.

6. (Original) The dual bank FIFO memory buffer of claim 5, wherein each write pointer is operable to control write access to its associated FIFO bank.

7. (Original) The dual bank FIFO memory buffer of claim 6, wherein write access is granted via write pointer only during predetermined time periods when the read data is determined to be valid.

8. (Original) The dual bank FIFO memory buffer of claim 7, wherein determination that the read data is valid comprises determination that a programmed expected time delay after issuing a read request has occurred.

9. (Original) The dual bank FIFO memory buffer of claim 8, wherein the programmed expected time delay is determined independently for different units of memory.

10. (Previously Amended) A dual bank FIFO memory buffer, comprising:

a first bank of memory elements operable to buffer memory data;

a second bank of memory elements operable to buffer memory data;

write control address logic operable to store selected memory data in memory elements with selected addresses, the selected addresses determined by evaluation of a strobe signal;

write control timing logic operable to selectively grant write access to the banks of memory elements at predetermined time, the write control timing logic comprising a write pointer associated with each FIFO bank and operable to control write access to the associated bank during periods when read data is determined to be valid;

read control logic operable to read data stored in the first and second banks;

a first port connecting the dual bank FIFO memory buffer to a memory; and

a second port connecting the dual bank FIFO memory buffer to a memory controller.

11. (Presently Amended) A memory controller, comprising:

a command signal output operable to issue a data read command;

a data input operable to receive read data from a memory; and

a dual-bank FIFO connected between the data input and the memory and operable to buffer the read data, the dual-bank FIFO further comprising:

a first bank of memory elements operable to buffer memory data;

a second bank of memory elements operable to buffer memory data;

write control address logic operable to store selected memory data in memory elements with selected addresses;

a first write pointer associated with the first bank of memory elements, the first write pointer operable to allow received data to be written to the first bank of memory elements when a second write pointer is in a null state;

a second write pointer associated with the second bank of memory elements, the second write pointer operable to allow received data to be written to the second bank of memory elements when the first write pointer is in a null state;

write control timing logic operable to selectively grant write access to the banks of memory elements at predetermined times by enabling the first and second write pointers at times dependent on received strobe signal preamble timing; and

read control logic operable to read data stored in the first and second banks.

12. (Original) The memory controller of claim 11, wherein the memory data is provided by double data rate synchronous dynamic read only memory (DDR SDRAM) operatively connected to the buffer.

13. (Original) The memory controller of claim 11, wherein the write control address logic is operable to determine an element within a bank of memory elements in which selected memory data is to be stored by evaluating rising and falling edges of a strobe signal.

14. (Original) The memory controller of claim 13, wherein the determination of the element in which selected memory data is to be stored further comprises selection of sequential element addresses during sequential strobe cycles.

15. (Original) The memory controller of claim 11, wherein the write control timing logic comprises a write pointer associated with each FIFO bank.

16. (Original) The memory controller of claim 15, wherein each write pointer is operable to control write access to its associated FIFO bank.

17. (Original) The memory controller of claim 16, wherein write access is granted via write pointer only during predetermined time periods when the read data is determined to be valid.

18. (Original) The memory controller of claim 17, wherein determination that the read data is valid comprises determination that a programmed expected time delay after issuing a read request has occurred.

19. (Original) The memory controller of claim 18, wherein the programmed expected time delay

is determined independently for different units of memory.

20. (Presently Amended) A computerized information handling system, the system comprising:

a memory controller;

a memory;

a processor; and

a dual-bank FIFO connected between the memory and the memory controller and operable to buffer read data, the dual-bank FIFO further comprising:

a first bank of memory elements operable to buffer memory data;

a second bank of memory elements operable to buffer memory data;

write control address logic operable to store selected memory data in memory elements with selected addresses;

a first write pointer associated with the first bank of memory elements, the first write pointer operable to allow received data to be written to the first bank of memory elements when a second write pointer is in a null state;

a second write pointer associated with the second bank of memory elements, the second write pointer operable to allow received data to be written to the second bank of memory elements when the first write pointer is in a null state;

write control timing logic operable to selectively grant write access to the banks of memory elements at predetermined times by enabling the first and second write pointers at times dependent on received strobe signal preamble timing; and

read control logic operable to read data stored in the first and second banks.

21. (Original) The dual bank FIFO memory buffer of claim 1, wherein the memory data is provided by double data rate synchronous dynamic read only memory (DDR SDRAM) operatively connected to the buffer.

22. (Original) The dual bank FIFO memory buffer of claim 20, wherein the write control address logic is operable to determine an element within a bank of memory elements in which selected memory data is to be stored by evaluating rising and falling edges of a strobe signal.

23. (Original) The dual bank FIFO memory buffer of claim 22, wherein the determination of the element in which selected memory data is to be stored further comprises selection of sequential element addresses during sequential strobe cycles.

24. (Original) The dual bank FIFO memory buffer of claim 20, wherein the write control timing logic comprises a write pointer associated with each FIFO bank.

25. (Original) The dual bank FIFO memory buffer of claim 24, wherein each write pointer is operable to control write access to its associated FIFO bank.

26. (Original) The dual bank FIFO memory buffer of claim 25, wherein write access is granted via write pointer only during predetermined time periods when the read data is determined to be valid.

27. (Original) The dual bank FIFO memory buffer of claim 26, wherein determination that the read data is valid comprises determination that a programmed expected time delay after issuing a read request has occurred.

28. (Original) The dual bank FIFO memory buffer of claim 27, wherein the programmed expected time delay is determined independently for different units of memory.

29. (Previously Amended) A method of compensating for potential read loop delay timing-induced read errors, comprising:

selectively granting write access to a bank of FIFO buffer memory selected from a multi-bank FIFO of memory elements at determined time via write control timing logic, the write control timing logic comprising a write pointer associated with each FIFO bank and operable to control write access to the associated bank during periods when read data is determined to be valid, the multi-bank FIFO coupled between a memory and a memory controller.